Amendments to the Claims:

Claim 1 (original): An extreme ultraviolet (EUV) lithographic mask comprising:

a substrate;

a first reflectance region overlying said substrate; and

an attenuating phase shifter overlying said first reflectance region, wherein a plurality of openings through said attenuating phase shifter expose portions of said first reflectance region and wherein said attenuating phase shifter attenuates EUV radiation through a combination of absorption and destructive interference.

Claim 2 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 1 wherein said attenuating phase shifter comprises:

an embedded layer overlying said first reflectance region;

a second reflectance region overlying said embedded layer; and

an absorber layer overlying said embedded layer.

Claim 3 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 2 wherein said embedded layer is an etch stop for etching said plurality of openings through said attenuating phase shifter.

Claim 4 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 3 wherein said embedded layer is optically tuned for destructive interference to attenuate EUV thereby minimizing a stack height of said embedded layer, said second reflectance region, and said absorber layer.

Claim 5 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 4 wherein said first and second reflectance regions comprise multilayer thin films for reflecting EUV radiation.

Claim 6 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 5 wherein said first and second reflectance regions comprise alternating thin film layers of molybdenum and silicon.

Claim 7 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 6 wherein a period of said first and second reflectance region has a thickness approximately equal to a half of the wavelength of EUV radiation that is directed at the EUV lithographic mask for patterning a semiconductor substrate.

Claim 8 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 4 wherein said embedded layer comprises NiFe.

Claim 9 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 4 wherein said absorber layer comprises TaN.

Claim 10 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 4 wherein said substrate comprises a LTEM (low thermal expansion material).

Claim 11 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 4 wherein a total stack height of said embedded layer, said second reflectance region, and said absorber layer is less than 700 angstroms.

Claim 12 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 11 wherein EUV radiation reflected from said embedded layer, said second reflectance region, and said absorber layer is phase shifted approximately 180 degrees out of phase to EUV radiation reflected from said first reflectance region.

Claim 13 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 12 wherein said embedded layer comprises a layer of NiFe approximately 27 angstroms thick.

Claim 14 (original): The extreme ultraviolet (EUV) lithographic mask as recited in claim 13 wherein said absorber layer comprises approximately 292 angstroms of TaN and wherein said second reflectance region comprises 7 periods of molybdenum and silicon.

Claim 15 (original): A method of manufacturing an integrated circuit comprising the steps of:

projecting radiation having a wavelength less than 40 nanometers towards a mask having a plurality of openings through an attenuating phase shifter, said plurality of openings expose a reflectance region in said mask wherein said attenuating phase shifter is less than 700 angstroms thick;

reflecting radiation impinging on said reflectance region exposed by said plurality of openings; and

attenuating and phase shifting radiation impinging on said attenuating phase shifter wherein said attenuating phase shifter attenuates radiation through destructive interference and absorption.

Claim 16 (original): The method of manufacturing an integrated circuit as recited in claim 15 further including a step of directing radiation reflected from said mask to a semiconductor wafer.

Claim 17 (original): The method of manufacturing an integrated circuit as recited in claim 16 wherein said step of attenuating and phase shifting radiation impinging on said attenuating phase shifter wherein said attenuating phase shifter attenuates radiation through destructive interference and absorption further includes a step of using an approximately 27 angstrom layer of NiFe in said attenuating phase shifter to destructively interfere with radiation impinging thereon.

Claim 18 (original): The method of manufacturing an integrated circuit as recited in claim 16 further including the steps of:

exposing photoresist on a surface of said semiconductor wafer with radiation reflected from said mask;

removing some of said photoresist corresponding to photoresist exposed by radiation reflected from said mask to form a pattern of photoresist on said surface of said semiconductor wafer; and

using said pattern of photoresist to form devices and interconnect of the integrated circuit.

Claim 19 (original): The method of manufacturing an integrated circuit as recited in claim 15 wherein said step of attenuating and phase shifting radiation impinging on said attenuating phase shifter wherein said attenuating phase shifter attenuates radiation through destructive interference and absorption further includes a step of providing an attenuating phase shifter comprising an embedded layer, a second reflectance region, and an absorber layer.

Claim 20 (original): The method of manufacturing an integrated circuit as recited in claim 19 further including a step of using said embedded layer as an etch stop for etching said plurality of openings through said attenuating phase shifter.

Claim 21 (original): The method of manufacturing an integrated circuit as recited in claim 19 further including a step of using a multilayer thin film for said second reflectance region.

Claim 22 (original): The method of manufacturing an integrated circuit as recited in claim 19 using alternating layers of molybdenum and silicon in said second reflectance region.

Claim 23 (original): The method of manufacturing an integrated circuit as recited in claim 19 using a period in said reflectance region and said second reflectance region substantially equal to a half of the wavelength of the projected EUV radiation.

Claim 24 (original): The method of manufacturing an integrated circuit as recited in claim 19 further including a step of shifting EUV radiation reflected from said attenuating phase shifter 180 degrees out of phase with EUV radiation reflected from said reflectance region.

Claim 25 (original): The method of manufacturing an integrated circuit as recited in claim 15 further including a step of supporting said reflectance region and said attenuating phase shifter with a low thermal expansion substrate.

Claim 26 (original): The method of manufacturing an integrated circuit as recited in claim 19 further including a step of using 7 periods of molybdenum and silicon as said second reflectance region.

Claim [[28]] 27. (currently amended) The method of manufacturing an integrated circuit as recited in claim 19 further including a step of using a layer of TaN approximately 292 angstroms thick as said absorber layer.

Claim [[29]] 28. (currently amended) A method of forming an extreme ultraviolet (EUV) mask for reflecting radiation having a wavelength less than 40 nanometers comprising the steps of:

providing a substrate;

forming a first reflectance region overlying said substrate;

forming an attenuating phase shifter overlying said first reflectance region wherein said attenuating phase shifter attenuates EUV radiation through a combination of destructive interference and absorption and wherein said attenuating phase shifter is less than 700 angstroms thick; and

forming a plurality of openings through said attenuating phase shifter to expose said first reflectance region.

Claim [[30]] 29. (currently amended) The method of forming an extreme ultraviolet (EUV) mask as recited in claim [[29]] 28 wherein said step of forming an attenuating phase shifter overlying said first reflectance region wherein said attenuating phase shifter attenuates EUV radiation through a combination of destructive interference and absorption and wherein said attenuating phase shifter is less than 700 angstroms thick further includes the steps of:

forming an embedded layer overlying said first reflectance region, said embedded layer being tuned to destructively interfere with EUV radiation;

forming a second reflectance region overlying said embedded layer; and

forming an absorber layer overlying said second reflectance region wherein said embedded layer acts as an etch stop when forming said plurality of openings.